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FLOW AND HEAT TRANSFER PROBLEMS IN THE SEMICONDUCTOR MANUFACTURING PROCESSES

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ABBREVIATION

CVD	chemical vapor deposition
DRAM	dynamic random access memory
DSMC	direct simulation Monte Carlo (method)
IC	integrated circuit
ULSI	ultra large scale integration

ABSTRACT

The integrated circuit (IC) market has been growing rapidly recently with factory sales increasing by an average 20% per year. By the year 2000, it may surpass the automobile, chemical, and steel industries in sales volume. The number of components per IC chips, developed in 1959, grow exponentially year by year. Now ultra large scale integration (ULSI) devices in which components exceed 1,000,000 are produced. Dynamic random access memory (DRAM) has increased the integration by four times in three years. The 4 M (megabit)DRAM and 16 MDRAM are produced in mass production, 64 MDRAM is shipped as samplers, and 256 MDRAM is developed in the laboratory. As chips become more integrated, their line widths (device feature size) are being reduced to submicron dimensions to decrease the cost per bit. Mechanical engineers began to participate in the development of ICs and manufacturing equipment after around 1980 to optimize the processes and the reactors.

A main theme in the IC industry is the simultaneous fabrication of hundreds of ICs (or chips) on a wafer of silicon, which is typically 100-200 mm in diameter and 1-mm thick. The wafer size increases as the device feature size decreases. Many individual process steps, which are precisely controlled and carefully sequenced, are required for the fabrication. ICs are built-up from layers of film conducting, insulating, and semiconducting films. Each film has a pattern etched into it so that an exactly registered array of these layers forms individual components such as transistors, resistors, diodes, and capacitors. These components are interconnected by conducting films to yield circuits. Uniformity of these films in device feature size and wafer size is required for the high throughput of chips. Even 1-μm particulates decrease the yield of chips if they adhere to wafers during manufacturing. Many efforts have been made to eliminate the particulate contamination in the manufacturing processes.

Unit operations in semiconductor manufacturing are
Bulk crystal growth by the Czochralski method,
Chemical reactions with surfaces (Etching, Oxidation),
Thin-film formation (Sputtering, CVD, Spin coating),
Lithography,
Semiconductor doping (Diffusion, Ion implantation),
Other new techniques.

Many problems of flow and heat transfer are found in these processes. These problems are found in two groups of wafer size (a few hundred mm order) and device feature size (μm order). The former is the flow in the manufacturing equipment and the latter is the flow around the submicron trench or holes on the wafers. The control of flow velocity, concentration, and temperature distribution was designed and executed precisely to keep the uniformity of the layers in both sizes. The flows in the CVD reactors show complex phenomena including chemical reactions with the particle contamination. Plasma is often used in the CAD during the lower temperature process and in etching for the smaller scale process. New high-density-plasma reactors have been developed and competed in the market.

With the trend towards finer line structures on chips, deposition profiles in small trenches suffer from poor step-coverage. Since poor step-coverage affects production yield and device reliability, several counter-measures have been taken to improve it. The flow and deposition in low-pressure apparatus and around submicron trenches are analyzed as rarefied gas flow using the DSMC method.